MICROCHIP

TC429

6A Single High-Speed, CMOS Power MOSFET Driver

Features

- High Peak Output Current: 6A
- Wide Operating Range: 7V to 18V
- High Impedance CMOS Logic Input
- Logic Input Threshold Independent of Supply Voltage
- Low Supply Current
  - With Logic 1 Input – 5mA Max
  - With Logic 0 Input – 0.5mA Max
- Output Voltage Swing Within 25mV of Ground or V_{DD}
- Short Delay Time: 75nsec Max
- High Capacitive Load Drive Capability
  - t_{RISE}, t_{FALL} = 35nsec Max With C_{LOAD} = 2500pF

Applications

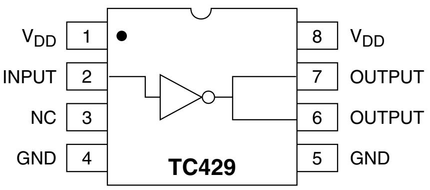
- Switch-Mode Power Supplies
- CCD Drivers
- Pulse Transformer Drive
- Class D Switching Amplifiers

Device Selection Table

Part Number	Package	Temp. Range
TC429CPA	8-Pin PDIP	0°C to +70°C
TC429EPA	8-Pin PDIP	-40°C to +85°C
TC429MJA	8-Pin CERDIP	-55°C to +125°C

Package Type

8-Pin PDIP/CERDIP



NC = No internal connection

NOTE: Duplicate pins must both be connected for proper operation.

General Description

The TC429 is a high-speed, single CMOS-level translator and driver. Designed specifically to drive highly capacitive power MOSFET gates, the TC429 features 2.5Ω output impedance and 6A peak output current drive.

A 2500pF capacitive load will be driven 18V in 25nsec. The rapid switching times with large capacitive loads minimize MOSFET transition power loss.

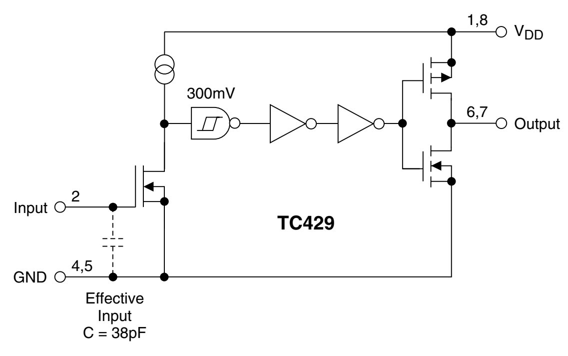
A TTL/CMOS input logic level is translated into an output voltage swing that equals the supply and will swing to within 25mV of ground or V_{DD}. Input voltage swing may equal the supply. Logic input current is under 10µA, making direct interface to CMOS/bipolar switch-mode power supply controllers easy. Input “speed-up” capacitors are not required.

The CMOS design minimizes quiescent power supply current. With a logic 1 input, power supply current is 5mA maximum and decreases to 0.5mA for logic 0 inputs.

For dual devices, see the TC426/TC427/TC428, TC4426/TC4427/TC4428 and TC4426A/TC4427A/TC4428A data sheets.

For noninverting applications, or applications requiring latch-up protection, see the TC4420/TC4429 data sheet.

Typical Application



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings*

Supply Voltage	+20V
Input Voltage, Any Terminal	V_{DD} + 0.3V to GND – 0.3V
Power Dissipation ($T_A \le 70°C$)	
PDIP	730mW
CERDIP	800mW
Derating Factor	
PDIP	5.6mW/°C Above 36°C
CERDIP	6.4mW/°C
Operating Temperature Range	
C Version	0°C to +70°C
E Version	-40°C to +85°C
M Version	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operation sections of the specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

TC429 ELECTRICAL SPECIFICATIONS

Electrical Characteristics: T_A = +25°C with 7V $\le V_{DD} \le$ 18V, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input						
V_{IH}	Logic 1, High Input Voltage	2.4	1.8	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	1.3	0.8	V	
I_{IN}	Input Current	-10	—	10	µA	$0V \le V_{IN} \le V_{DD}$
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	
V_{OL}	Low Output Voltage	—	—	0.025	V	
R_O	Output Resistance	—	1.8	2.5	Ω	V_{IN} = 0.8V, I_{OUT} = 10mA, V_{DD} = 18V
		—	1.5	2.5	Ω	V_{IN} = 2.4V, I_{OUT} = 10mA, V_{DD} = 18V
I_{PK}	Peak Output Current	—	6	—	A	V_{DD} = 18V (Figure 3-4)
Switching Time (Note 1)						
t_R	Rise Time	—	23	35	nsec	Figure 3-1, C_L = 2500pF
t_F	Fall Time	—	25	35	nsec	Figure 3-1, C_L = 2500pF
t_{D1}	Delay Time	—	53	75	nsec	Figure 3-1
t_{D2}	Delay Time	—	60	75	nsec	Figure 3-1
Power Supply						
I_S	Power Supply Current	— —	3.5 0.3	5 0.5	mA	V_{IN} = 3V V_{IN} = 0V

Note 1: Switching times ensured by design.

TC429 ELECTRICAL SPECIFICATIONS (CONTINUED)

Electrical Characteristics: Over operating temperature range with $7V \le V_{DD} \le 18V$, unless otherwise noted.						
Symbol	**Parameter**	**Min**	**Typ**	**Max**	**Units**	**Test Conditions**
Input						
V_{IH}	Logic 1, High Input Voltage	2.4	—	—	V	
V_{IL}	Logic 0, Low Input Voltage	—	—	0.8	V	
I_{IN}	Input Current	-10	—	10	µA	$0V \le V_{IN} \le V_{DD}$
Output						
V_{OH}	High Output Voltage	V_{DD} – 0.025	—	—	V	
V_{OL}	Low Output Voltage	—	—	0.025	V	
R_O	Output Resistance	—	—	5	Ω	V_{IN} = 0.8V, I_{OUT} = 10mA, V_{DD} = 18V
		—	—	5	Ω	V_{IN} = 2.4V, I_{OUT} = 10mA, V_{DD} = 18V
Switching Time (Note 1)						
t_R	Rise Time	—	—	70	nsec	Figure 3-1, C_L = 2500pF
t_F	Fall Time	—	—	70	nsec	Figure 3-1, C_L = 2500pF
t_{D1}	Delay Time	—	—	100	nsec	Figure 3-1
t_{D2}	Delay Time	—	—	120	nsec	Figure 3-1
Power Supply						
I_S	Power Supply Current	— —	— —	12 1	mA	V_{IN} = 3V V_{IN} = 0V

Note 1: Switching times ensured by design.

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin No. (8-Pin PDIP, CERDIP)	Symbol	Description
1	V_{DD}	Supply input, 7V to 18V.
2	INPUT	Control input, TTL/CMOS compatible logic input.
3	NC	No connection.
4	GND	Ground.
5	GND	Ground.
6	OUTPUT	CMOS totem-pole output, common to Pin 7.
7	OUTPUT	CMOS totem-pole output, common to Pin 6.
8	V_{DD}	Supply input, 7V to 18V.

3.0 APPLICATIONS INFORMATION

3.1 Supply Bypassing

Charging and discharging large capacitive loads quickly requires large currents. For example, charging a 2500pF load to 18V in 25nsec requires a 1.8A current from the device's power supply.

To ensure low supply impedance over a wide frequency range, a parallel capacitor combination is recommended for supply bypassing. Low-inductance ceramic disk capacitors with short lead lengths (< 0.5 in.) should be used. A 1µF film capacitor in parallel with one or two 0.1µF ceramic disk capacitors normally provides adequate bypassing.

3.2 Grounding

The high-current capability of the TC429 demands careful PC board layout for best performance. Since the TC429 is an inverting driver, any ground lead impedance will appear as negative feedback which can degrade switching speed. The feedback is especially noticeable with slow rise-time inputs, such as those produced by an open-collector output with resistor pull-up. The TC429 input structure includes about 300mV of hysteresis to ensure clean transitions and freedom from oscillation, but attention to layout is still recommended.

Figure 3-3 shows the feedback effect in detail. As the TC429 input begins to go positive, the output goes negative and several amperes of current flow in the ground lead. As little as 0.05Ω of PC trace resistance can produce hundreds of millivolts at the TC429 ground pins. If the driving logic is referenced to power ground, the effective logic input level is reduced and oscillations may result.

To ensure optimum device performance, separate ground traces should be provided for the logic and power connections. Connecting logic ground directly to the TC429 GND pins ensures full logic drive to the input and fast output switching. Both GND pins should be connected to power ground.

FIGURE 3-1: INVERTING DRIVER SWITCHING TIME TEST CIRCUIT

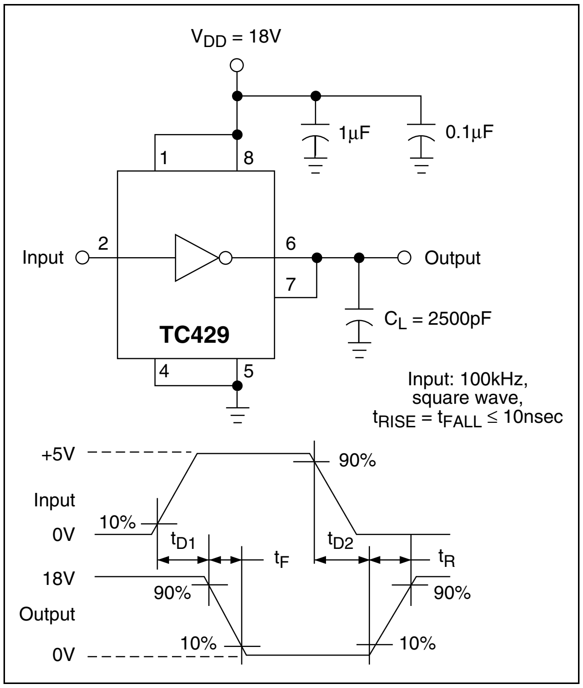


FIGURE 3-2: SWITCHING SPEED

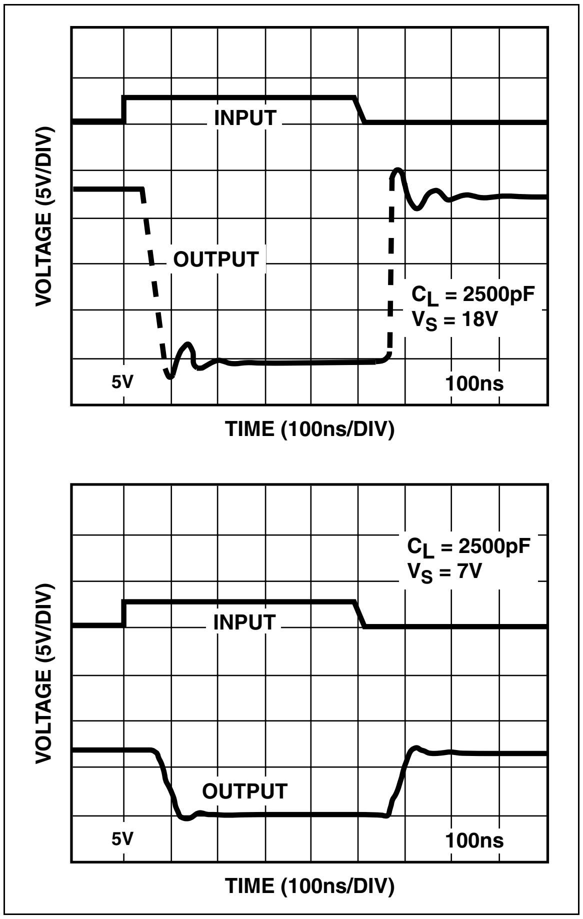
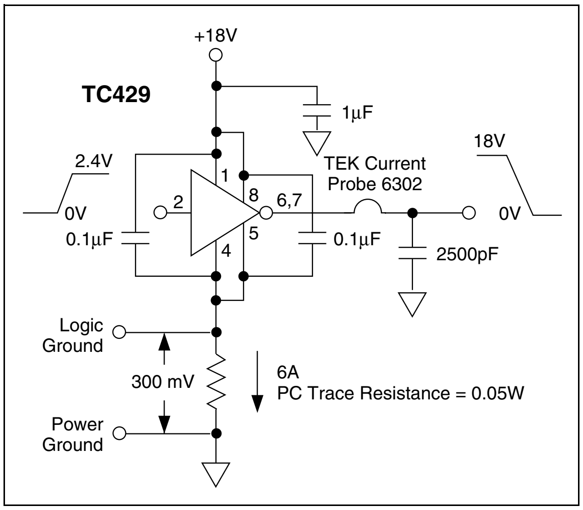


FIGURE 3-3: SWITCHING TIME DEGRADATION DUE TO NEGATIVE FEEDBACK



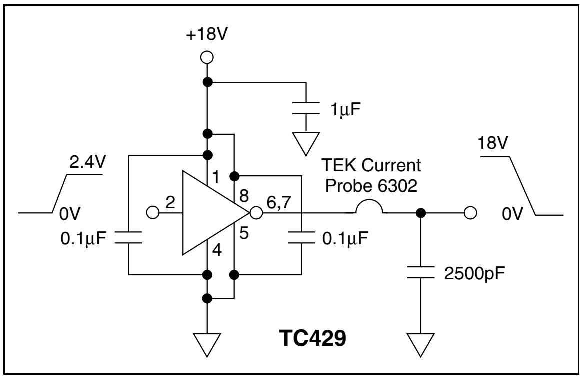
3.3 Input Stage

The input voltage level changes the no-load or quiescent supply current. The N-channel MOSFET input stage transistor drives a 3mA current source load. With a logic “1” input, the maximum quiescent supply current is 5mA. Logic “0” input level signals reduce quiescent current to 500µA maximum.

The TC429 input is designed to provide 300mV of hysteresis, providing clean transitions and minimizing output stage current spiking when changing states. Input voltage levels are approximately 1.5V, making the device TTL compatible over the 7V to 18V operating supply range. Input current is less than 10µA over this range.

The TC429 can be directly driven by TL494, SG1526/1527, SG1524, SE5560 or similar switch-mode power supply integrated circuits. By off-loading the power-driving duties to the TC429, the power supply controller can operate at lower dissipation, improving performance and reliability.

FIGURE 3-4: PEAK OUTPUT CURRENT TEST CIRCUIT



3.4 Power Dissipation

CMOS circuits usually permit the user to ignore power dissipation. Logic families such as the 4000 and 74C have outputs that can only supply a few milliamperes of current, and even shorting outputs to ground will not force enough current to destroy the device. The TC429, however, can source or sink several amperes and drive large capacitive loads at high frequency. The package power dissipation limit can easily be exceeded. Therefore, some attention should be given to power dissipation when driving low impedance loads and/or operating at high frequency.

The supply current versus frequency and supply current versus capacitive load characteristic curves will aid in determining power dissipation calculations. Table 3-1 lists the maximum operating frequency for several power supply voltages when driving a 2500pF load. More accurate power dissipation figures can be obtained by summing the three power sources.

Input signal duty cycle, power supply voltage and capacitive load influence package power dissipation. Given power dissipation and package thermal resistance, the maximum ambient operation temperature is easily calculated. The 8-pin CERDIP junction-to-ambient thermal resistance is 150°C/W. At +25°C, the package is rated at 800mW maximum dissipation. Maximum allowable chip temperature is +150°C.

Three components make up total package power dissipation:

- Capacitive load dissipation (P_C)
- Quiescent power (P_Q)
- Transition power (P_T)

The capacitive load-caused dissipation is a direct function of frequency, capacitive load and supply voltage.

The package power dissipation is:

$$P_C = f\,C\,V_S^2$$

Where:

f = Switching frequency
C = Capacitive load
V_S = Supply voltage

Quiescent power dissipation depends on input signal duty cycle. A logic low input results in a low-power dissipation mode with only 0.5mA total current drain. Logic high signals raise the current to 5mA maximum.

The quiescent power dissipation is:

$$P_Q = V_S\,(D\,(I_H) + (1 - D)\,I_L)$$

Where:

I_H = Quiescent current with input high (5mA max)
I_L = Quiescent current with input low (0.5mA max)
D = Duty cycle

Transition power dissipation arises because the output stage N- and P-channel MOS transistors are ON simultaneously for a very short period when the output changes.

The transition package power dissipation is approximately:

$$P_T = f\,V_S\,(3.3 \times 10^{-9}\ \text{A} \bullet \text{Sec})$$

An example shows the relative magnitude for each item.

C = 2500pF
V_S = 15V
D = 50%
f = 200kHz
P_D = Package power dissipation = $P_C + P_T + P_Q$
= 113mW + 10mW + 41mW
= 164mW

Maximum operating temperature = $T_J - \theta_{JA}\,(P_D)$
= 125°C

Where:

T_J = Maximum allowable junction temperature (+150°C)
θ_{JA} = Junction-to-ambient thermal resistance (150°C/W, CERDIP)

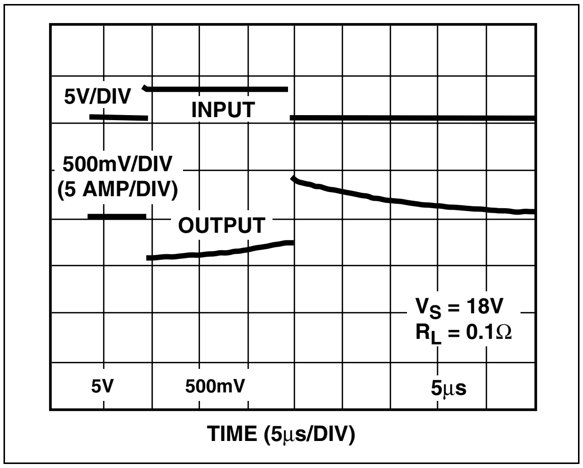
Note: Ambient operating temperature should not exceed +85°C for IJA devices or +125°C for MJA devices.

TABLE 3-1: MAXIMUM OPERATING FREQUENCIES

V_S	f_{MAX}
18V	500kHz
15V	700kHz
10V	1.3MHz
5V	>2MHz

CONDITIONS: 1. CERDIP Package (θ_{JA} =150°C/W)
2. T_A = +25°C
3. C_L = 2500pF

FIGURE 3-5: PEAK OUTPUT CURRENT CAPABILITY



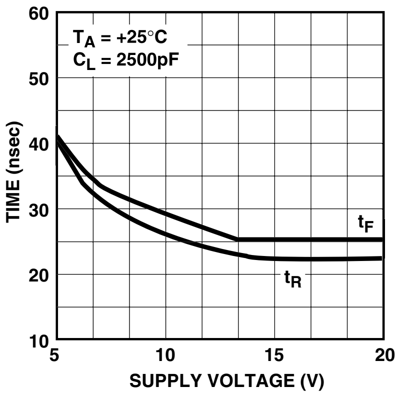
3.5 POWER-ON OSCILLATION

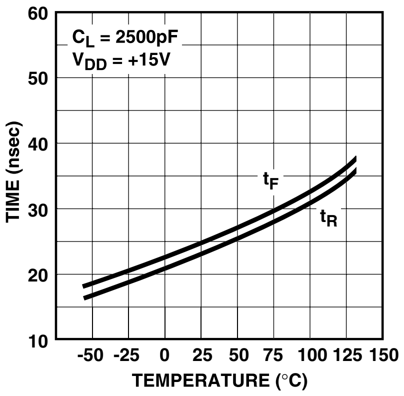
Note: It is extremely important that all MOSFET Driver applications be evaluated for the possibility of having High-Power Oscillations occurring during the power-on cycle.

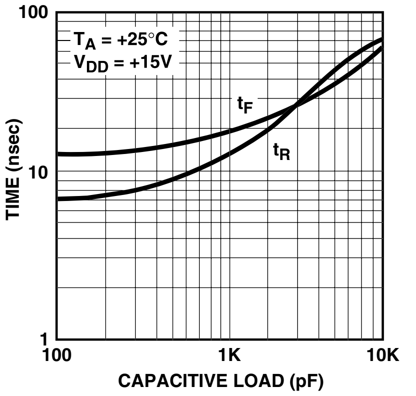
Power-on oscillations are due to trace size and layout as well as component placement. A 'quick fix' for most applications which exhibit power-on oscillation problems is to place approximately 10kΩ in series with the input of the MOSFET driver.

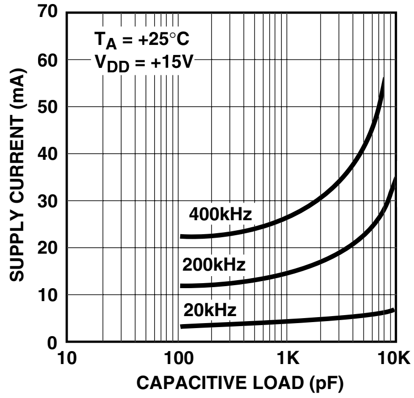
4.0 TYPICAL CHARACTERISTICS

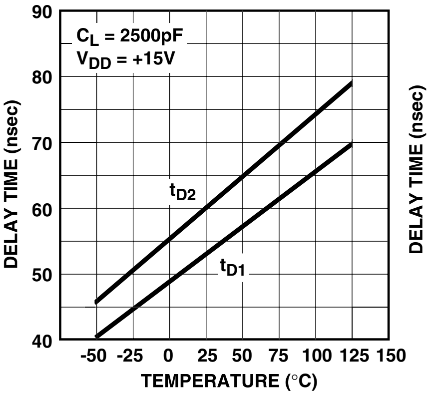
Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

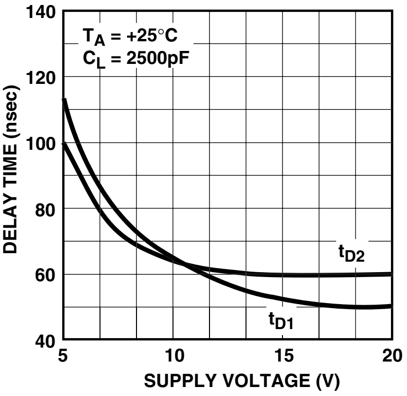

Rise/Fall Times vs. Supply Voltage

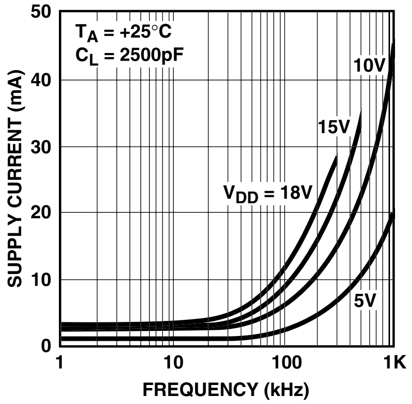

Rise/Fall Times vs. Temperature

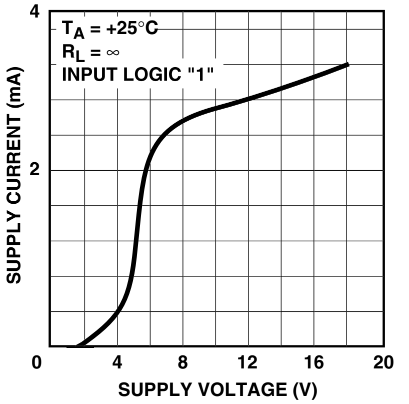

Rise/Fall Times vs. Capacitive Load

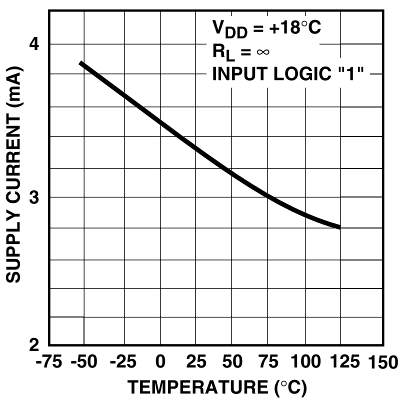

Supply Current vs. Capacitive Load


Delay Times vs. Temperature


Delay Times vs. Supply Voltage

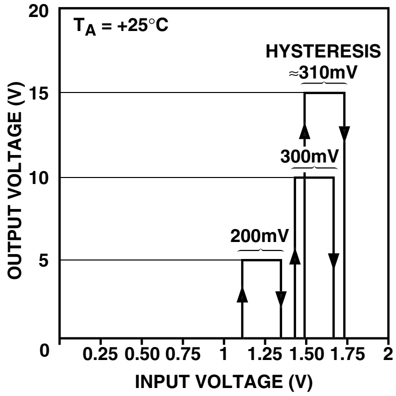

Supply Current vs. Frequency


Supply Current vs. Supply Voltage

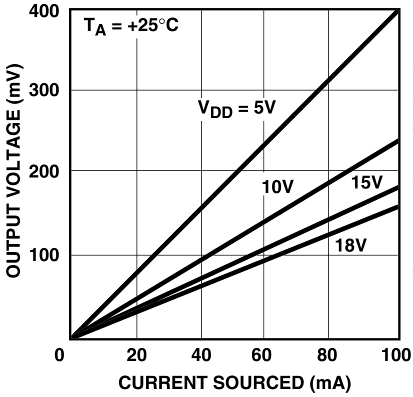

Supply Current vs. Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

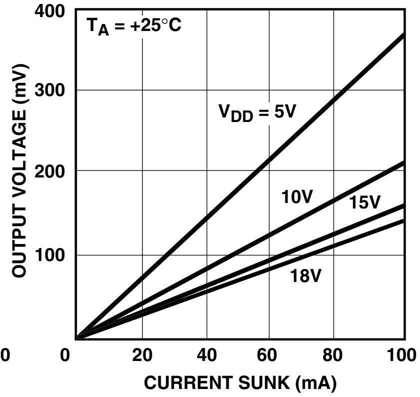
Voltage Transfer Characteristics



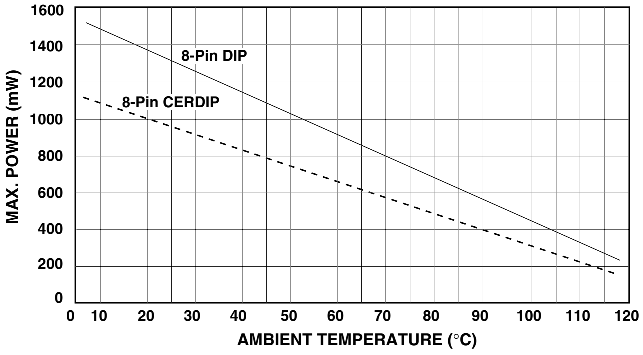
High Output Voltage vs. Current



Low Output Voltage vs. Current



Thermal Derating Curves



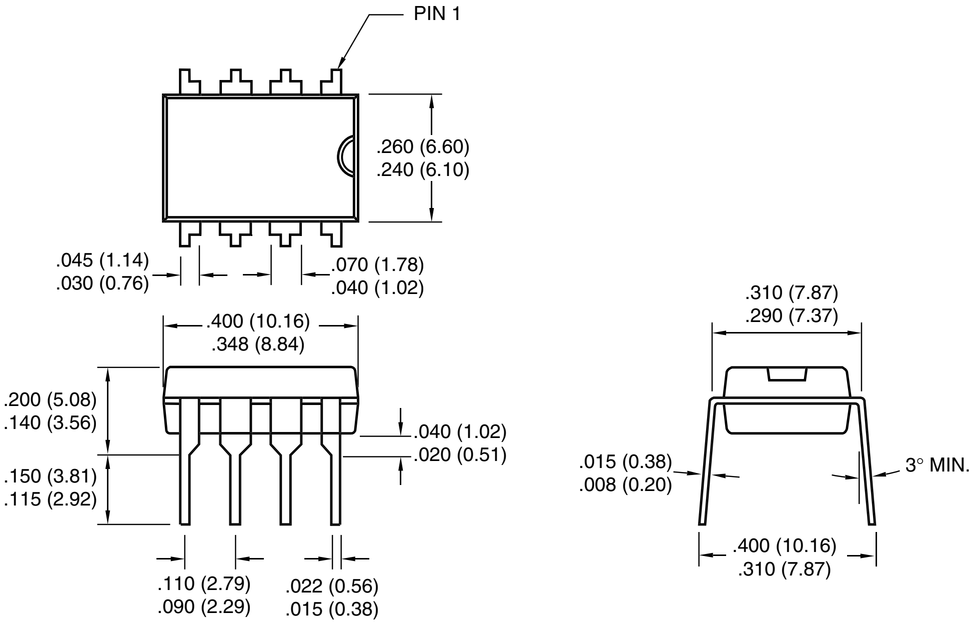
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

Package marking data not available at this time.

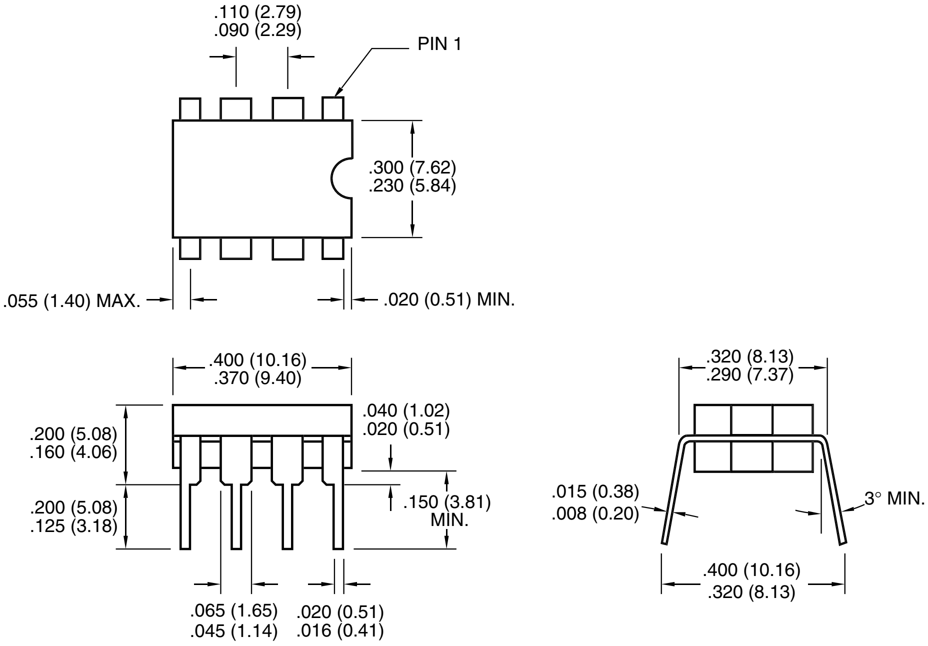
5.2 Package Dimensions

8-Pin Plastic DIP



Dimensions: inches (mm)

8-Pin CERDIP (Narrow)



Dimensions: inches (mm)

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03/01/02